

**Requirements For 2eVME & 2eSST-Compatible
Drivers, Receivers & Transceivers**

**VITA 2.1-199x Task Group
Working Document**

***** PRELIMINARY *****

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1. GENERAL INFORMATION

This document is intended as a preliminary working document for the VITA 2.1-199x Task Group. The purpose of the VITA 2.1-199x Task Group is to specify new ETL Transceivers for use in modules implementing VME64x (ANSI/VITA 1.1) 2eVME protocols and/or VITA 1.5-199x 2eSST protocols. The goal of defining these new components is such that modules using these new ETL components can reliably participate in either 2eVME or 2eSST operations at design speeds:

- a) in new VME64x and/or legacy backplane subracks
- b) under all module bus loading conditions
- c) with any mixture of old legacy modules and modules using these new ETL components within the subrack.

Simulations should tell whether all parts of this goal can be met. The document contains both justification for the VITA 2.1-199x ETL Transceiver specification and preliminary transceiver specifications for review.

1.1 VITA 2-199x

VITA 2-199x is currently being readied for ANSI balloting. When ETL transceivers compatible with that standard are used in modules implementing 2eVME protocols, some restrictions apply. Bandwidth of these protocols is limited over a 21-slot backplane. When using ETL transceivers compliant with the VITA 2-199x specification, a module can achieve maximum design speeds only in a backplane containing eight to ten slots. If, for example, passive components are used on each module to limit the load seen by drivers and to limit the driver rise and fall times, 21-slot 2eVME protocol operation is possible under certain loading conditions.

1.2 2eVME & 2eSST Protocols – Driver, Receiver & Transceiver Requirements

The following is a preliminary list of driver, receiver and transceiver requirements, subject to changes after simulations, which would be detailed in a new VITA 2.1-199x standard. These requirements would allow modules to implement 2eVME and 2eSST protocols that operate reliably in subracks with 21 or less slots and containing any mixture of VME64 and VME64x modules:

- 1) VITA 2-199x ETL receiver characteristics for receivers which would connect to the VME bus
- 2) Controlled four to five nanosecond rise and fall time drivers
- 3) Normal VME64x bus driver output current capabilities
- 4) Bias pin & circuitry for live insertion
- 5) Guaranteed and minimal output skew, pin to pin and IC to IC
- 6) Low output switching noise
- 7) Clocked or transparent input registers for optionally latching bus input signals
- 8) Surface mount and other packaged devices

1.3 Texas Instruments (TI) ETL ICs

Texas Instruments has a set of ICs called ABTE/ETL (Advanced BiCMOS Technology / Enhanced Transceiver Logic) ICs which are compatible to the VITA 2-199x standard. The set includes the SN54ABTE16245 and SN74ABTE16245, 16-bit and the SN74ABTE16246, 11-bit incident-wave switching bus transceivers with 3-state outputs and open-collector outputs. Under various loading conditions with 5-row P1 and P2 connectors and with a parallel 66 ohm resistor and 270 nanohenry inductor at each transceiver I/O pin, 2eVME protocols can operate in backplanes using these ETL devices. Refer to VITA 2-199x, draft 0.5, Appendix B or Section 2 of this document for further details.

1.4 Fairchild V320 ICs for Bustronics “Lumped-Capacity” Backplanes

Fairchild Semiconductor has produced a V320 8-Bit Registered Bus Transceiver for use with the Bustronics lumped-capacity backplane developed by Drew Berding of Arizona Digital. This device has two characteristics required for new VITA 2.1-199x compatible transceivers. The first is minimal pin to pin and IC to IC output skew and the second is low output switching noise. Without simulations, the maximum skew specifications of the V320 IC appear to be too large for non-lumped-capacity backplanes to support 2eVME and 2eSST protocols at design speeds.

2. Summary Of VSO's LLC Bus Simulation Studies

Appendix B of Draft 0.5 of VITA 2-199x (ETL) is included below to aid in understanding the need for a new ETL transceiver specification. This appendix summarizes the results of the bus simulations sponsored by VSO to aid in the final preparation of both the ANSI/VITA 1.1 (VME4x) and VITA 2-199x standards. This appendix gives additional details substantiating the comments at the end of Section 1.1 of this document regarding restrictions when using ETL components compliant with VITA 2-199x.

Appendix B of VITA 2-199x ETL ETL and 160 Pin Connector Simulation and Analysis Summary

Introduction

During the second half of 1996, 18 companies (see list of companies below) commissioned a simulation and analysis of the ETL devices and the 160 pin connector. The initial purpose of the simulation and analysis was to verify that ETL devices can generate incident waves when driving VME, VME64 and VME64x backplanes. The second goal was to find out how fast the backplane signals can be driven.

Phase One

The initial simulation showed that when ETL devices directly drive the VME, VME64 and VME64x backplanes, excessive near end and far end noise is generated in the connector. The noise from the combination of a large number of simultaneously switching signals, a limited number of grounds and a non optimized signal/ground connector pin assignment. Near end noise is noise that the driver boards see on undriven signal lines. Far end noise is noise that the receivers see on undriven signal lines. The simulation showed near end noise in the 2.0 volt range and far end noise in the 1.0 volt range, which is considered to be too high.

The initial simulation also showed that incident wave switching was not reliably achieved. Depending on bus loading configurations and other parameters, the bus settling time ranged from 11 to 14 nsec.

Phase Two - Slower is Faster

It was proposed to slow down the rise time, thereby making the backplane appear more "lumped" loaded rather than transmission line. A piece wise linear simulation was performed, using the approximate ETL driver impedance. 5 nsec rise and fall times yielded the best performance, where all the bus signals were monotonic rising or falling. No settling time was needed since the bus signal passed through the receiver threshold on the incident wave.

The near end noise was reduced to less than 500 mV and far end to less than 50 mV. The end to end transmission time remained in the 10 nsec range for a 21 slot backplane.

In effect, the bus signaling is much faster, since there is less noise, less settling time and the signal is ready for another transition soon after reaching the high or low state.

Dealing with Near End Noise

It was agreed upon by the VSO that excessive near end noise is to be handled by the bus interface logic. All bus input signals are to be heavily filtered or turned off when a board is driving the backplane. Noise returning from the connector on the undriven signals will cross the receiver threshold, thereby creating extraneous inputs. Most all existing VME interface logic already handle this situation. Reducing the near end noise to the point where the noise will not cause extraneous inputs, would cause a significant reduction in backplane performance.

Phase Three

With a target of 5 nsec rise and fall times, multiple filter circuits were simulated. The best ETL circuit for achieving the optimum between reasonable signal transition time and lowest connector noise is an in-line parallel

RL circuit of 66 ohms and 270 nH. This parallel circuit would be used on all driven and received bus signals and placed between the ETL device and the board's backplane connector.

With all boards containing the ETL + RL circuit, the worst case far end noise is in the 200 mV range. All signals are monotonically increasing or decreasing, with respect to the 1.4 V to 1.6 V ETL receiver threshold, thereby achieving incident wave switching. Low level ringing was below 650 mV. This was simulated for the nominal, strongest and weakest ETL driver devices.

Final Phase

The final simulation used a mixture of ETL and TTL boards with a variety of backplane loading configurations. All ETL boards contained the RL circuit. Some TTL boards were simulated with and some without the RL circuit. Most of the simulation configurations used the 160 pin connector. A few configurations used the 96 pin connector. Both 10 and 21 slot backplanes were simulated. The following conclusions were drawn from the simulation.

1. Using strictly ETL + RL circuit boards in fully and partially loaded backplanes, incident wave switching can be achieved, based on 1.4 V to 1.6 V ETL receiver thresholds. Worst case far end noise remained below 300 mV.
2. When mixing original VME boards with ETL + RL circuit boards, incident wave switching can only be achieved when driving from the ends of the backplane. This is for any combination of fully and partially loaded backplanes. The driving ETL + RL circuit board and receiving ETL + RL circuit board must be in one of the first five slots or in one of last five backplane slots. This is based on 1.4 V to 1.6 V ETL receiver thresholds.
3. When driving in the middle of the backplane in mixed VME and ETL + RL circuit boards, a worst case shelf of 7 nsec was observed. This is where the received signal crossed the receiver threshold, returned to the starting logic state and then crossed the receiver threshold again.
4. For the incident wave switching cases, the worst case skew between the strongest and weakest ETL bus transceivers and between rising and falling edges is 2 nsec. Whenever shelving occurred, the worst case skew between strongest and weakest ETL bus transceiver and between rising and falling edges is 9 nsec. The 5% tolerance on the resistor and inductor has negligible effect on the rise and fall time values, including the skew numbers. Board trace length variation of up to 10 mm will also have negligible effect on skew.
5. When the bus is driven with ETL + RL boards, the maximum far end noise on receiving TTL boards with no filter is in the 900 mV range. This far end noise can be reduced to 450 mV when the RL circuit is incorporated on the TTL board.
6. The existing VME backplanes can be used **AS IS**. No changes need to be made to the electrical characteristics of VME, VME64 and VME64x backplanes. This includes the termination network of 330 over 470 ohm termination network.
7. ETL receiver thresholds of 1.4 V to 1.6 V provide a significant noise margin improvement over TTL receivers as well as improved consistency when the receiver switches on both high and low going signals. Low level noise is more problematic than high level noise. The added 600 mV of ETL noise margin is a significant improvement over TTL devices.
8. A bus transfer rate of 20 Mt/sec (mega-transfers) (a data beat every 50 nsec) can be achieved from a bus signaling point of view.
9. For new designs, it is highly recommended that the RL circuit be used on both ETL and TTL boards.

10. It is anticipated that the EMC radiation generated within VME computers will correspondingly be reduced as a result of slower edges produced by the parallel RL circuits in each bus signal line.

Side Bar

The simulated connector noise is truly worst-case. The simulations assumed all active signals switched at exactly the same instant. In reality, differing stub lengths and gate delays cause signals to reach the connector at slightly different times. This will tend to reduce noise amplitudes but increase pulse duration.

5% resister and inductors should be used in the above defined circuit.

Copies of the Simulation and Analysis Reports

Copies of the SOW (statement of work) and the four reports can be purchased from VITA.

Companies Supporting the Original Simulation

The following companies made financial contribution and personnel support for the above simulation: AirNet Communications, AMP, Cetia, CSPI, Dialogic, Digital Equipment Corporation, DY 4 Systems, Electronic Solutions, FermiLab, FORCE COMPUTERS, Harting, Hughes Aircraft Company, Hybricon, Motorola, TreNew Electronics, Tundra, VERO Electronics and VITA

Requirements

The following recommendations and rules are helpful if recommended RL circuit is incorporated on a VME, VME64 or VME64x board.

Recommendation B.1:

VME, VME64 and VME64x boards that incorporate ETL bus transceivers should use the parallel in-line RL (66 ohms, 270 nH, +/- 5%) circuit on each bus signal line between the ETL device and the backplane connector.

Recommendation B.2:

VME, VME64 and VME64x boards that incorporate TTL bus transceivers should use the in-line parallel RL (66 ohms, 270 nH, +/- 5%) on each bus signal line between the TTL bus transceiver and the backplane connector.

Rule B.1:

Whenever the RL circuit is used, the total trace distance for each bus signal between the backplane connector and the ETL or TTL device pin shall not exceed 37.5 mm.

Rule B.2:

Whenever the RL circuit is used, the trace distance between the backplane connector and the RL circuit shall not exceed 12.5 mm.

3. 2eVME & 2eSST Protocols – Driver & Receiver Preliminary Specifications

The following subsections include additional information regarding the requirements for new VITA 2.1-199x bus driver, receiver and/or transceiver integrated circuit(s). Specifications for driver, receiver and transceiver requirements below are based on Section 1.2.

3.1 VITA 2-199x ETL Receiver Compatible

The following table is a list of principal specifications from TI's series of VITA 2-199x ETL-compliant ICs. These should be part of the VITA 2.1-199x document. The specifications pertain to a receiver's incident wave switching ETL characteristics:

Mnemonic	Description	Value
V_{IH}	High-level input voltage	1.6 volts minimum
V_{OH}	Low-level input voltage	1.4 volts maximum
V_{HYS}	Input hysteresis	100 millivolts minimum

3.2 Output Drive Characteristics Including Controlled Rise & Fall Times

VSO sponsored simulations have shown that for 2eVME protocols to work at design speeds in 21-slot subracks with various combinations of and loading with VME64 and VME64x modules when the output driver rise and fall times are approximately 5 nanoseconds each.

3.3 Live Insertion Compatible

A pre-charge with identical functions to the V_{CCBIAS} pin in TI's series of VITA 2-199x ETL-compliant ICs is required in VITA 2.1-199x compliant ICs. Specifications for this feature in TI's ICs is given below:

live-insertion specifications over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	SN54ABTE16246			SN74ABTE16246			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
I_{CC} (V_{CCBIAS})		$V_{CC} = 0$ to 4.5 V, $V_{CCBIAS} = 4.5$ V to 5.5 V, $I_O(DC) = 0$		250	700		250	700	μA
		$V_{CC} = 4.5$ V to 5.5 V†, $V_{CCBIAS} = 4.5$ V to 5.5 V, $I_O(DC) = 0$			20			20	
V_O	A port	$V_{CC} = 0$							V
		$V_{CCBIAS} = 4.5$ V to 5.5 V	1.1	1.5	1.9	1.1	1.5	1.9	
		$V_{CCBIAS} = 4.75$ V to 5.25 V	1.3	1.5	1.7	1.3	1.5	1.7	
I_O	A port	$V_{CC} = 0$							μA
		$V_O = 0$, $V_{CCBIAS} = 4.5$ V	-20		-100	-20		-100	
		$V_O = 3$ V, $V_{CCBIAS} = 4.5$ V	20		100	20		100	

† All typical values are at $V_{CC} = 5$ V, $T_A = 25^\circ C$.

‡ $V_{CC} - 0.5$ V < V_{CCBIAS}

3.4 Minimal Output Skew – Pin To Pin & IC To IC

Specifications similar to the following list of principal Fairchild V320 IC specifications should be part of the VITA 2.1- 199x document. Simulations should be used to determine exact values for VITA 2.1-199x compatible devices.

These specifications pertain to pin to pin and IC to IC skew requirements:

Mnemonic	Skew	Time (Max.)	Output Load	Simultaneous Switching Outputs
t_{OSHL}	Output to output high to low	1.3 ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	8
t_{OSLH}	Output to output Low to high	1.1 ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	8
t_{pv}	Device to device	2.0 ns	$C_L = 50 \text{ pF}$ $R_L = 500 \Omega$	1

Notes:

- 1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device. The specification applies to outputs switching in the same direction also.
- 2) Device to device skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs from any two devices.

Editor's comments:

- 1) To properly specify t_{OSLH} and t_{OSHL} , output drive characteristics must be specified. The V320 IC specifies output switching for 50 pF, 250 pF and 500 pF loads. With controlled output rise and fall times, output drive characteristics in the VITA 2.1-199x will be different from those of the V320 IC which is specified to be able to drive relatively large capacitance loads.
- 2) The actual device to device skew of V320 ICs can be twice the value listed in the specifications. VITA 2.1-199x compatible devices will most probably require tighter skew specifications to be usable with 2eVME and 2eSST protocols over all loading conditions of modules in subracks. The device to device output skew of V320 devices is specified for one output switching whereas the ICs pin to pin output skew is specified for eight outputs switching. VITA 2.1-199x compatible devices will need to be specified for all outputs switching (worst case).

3.5 Low Output Switching Noise

The output switching noise for simultaneous switching of all VITA 2.1-199x compatible device outputs must be minimal and specified. Controlled rise and fall times should help minimize this noise. Simulations will be used to quantify this noise specification

3.6 Clocked Or Transparent Input Registers

VITA 2.1-199x compatible devices must be able of operating in a clocked mode. Given VITA 2.1-199x compatible devices with minimal input clock to output skew and operating in a clocked mode, the tight 2eSST bus protocol specifications will be more easily met.

4. Summary of Needed Simulations

Further simulations are needed to determine both the output driver and input receiver characteristics of VITA 2.1-199x compatible drivers necessary to support 2eVME and 2eSST protocols at maximum design speeds and under various conditions. Source, backplane and receiver skews must be thoroughly simulated to insure that they conform to that required to support 2eVME and 2eSST protocols at maximum design speeds. The following is an initial attempt to list the different combinations of parameters needing to be simulated to properly specify VITA 2.1-199x transceivers:

- 1) Various output driver input clock to output stable skew times pin to pin and IC to IC
- 2) Various output drive characteristics with various controlled rise and fall times
- 3) Various receiver input threshold sensitivity differences (minimum high-level input voltage to maximum low-level input voltage differential) and various absolute receiver input switching levels
- 4) Various receiver input clock to output stable skew times pin to pin and IC to IC
- 5) In legacy and VME64x backplanes, various bus loading conditions including various combinations of legacy and VITA 2.1-199x compatible modules and including the effects of different amounts of drivers and/or receivers on certain data and other signal lines (e.g., D08 modules mixed with D32 modules)
- 6) Acceptable simultaneous driver output switching noise for all the above variations device characteristics

Some reasonable subset of all the simulation possibilities given above will have to be decided upon so that a practical amount of simulations can be done to determine required device characteristics.

Editor's comments and questions:

- 1) Controlled and slower than usual rise and fall times might dictate smaller receiver input threshold sensitivity (minimum high-level input voltage to maximum low-level input voltage differential) specifications to insure reliable reception of data when 2eVME and especially 2eSST operations are occurring at the highest design speeds.
- 2) What is the range of controlled rise and fall times that can be maintained over the range of loading and receiver input threshold sensitivity?
- 3) Is it possible to only require the longer controlled rise and fall times during the worst loading conditions and still have 2eVME and 2eSST protocols work over 21 slots with any mixture of VITA 2.1-199x compatible and non-compatible ETL receivers on the bus and any distribution of bus loading?
- 4) Should this document consider listing a set of rules for maximum bus performance. If so, the rules could be more restrictive than the current VME standards. Some guidance to the designer of pitfalls that can occur when trying to maximize performance might be helpful. These should be listed in a way that does not denigrate current VME, but tells the user that this is a new "world" and more care is necessary.